

REMARKS

By this amendment, claims 1-11, 12-20, 22-31, and 33-36 have been amended. No new matter has been added. Claims 1-36 are pending in the application. Applicant reserves the right to pursue the original claims and other claims in this and other applications.

Claims 2-5, 7-9, 11-17, 19, 22-23, 25-30, 33-34, and 36 have been amended in minor fashion.

The title stands objected to as not being descriptive and has been amended to address the concerns raised in the Office Action. Applicant respectfully requests that the objection to the title be withdrawn.

The specification stands objected to for failing to provide proper antecedent basis for the claim 29 subject matter, "providing the reference voltage from the common operational amplifier-based charge sensing circuit." Claim 29 has been amended to address the concerns raised in the Office Action. Accordingly, Applicant respectfully requests that the objection to the specification be withdrawn.

Claims 18-19 and 28-30 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. The claims have been amended to address the concerns raised in the Office Action. Accordingly, Applicant respectfully requests that the rejection be withdrawn and the claims allowed.

Claims 1-2, 6, 10, 13-14, 16, 18, 20, 25-28, and 31 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Pain et al. (US WO 99/48281). This rejection is respectfully traversed.

Claim 1, as amended, recites an image sensor readout circuit comprising, *inter alia*, a “binning circuit [which] combines a predetermined plurality of analog pixel signals from a plurality of pixels and outputs them on a first output line, and combines a predetermined plurality of analog reset signals from a plurality of pixels and outputs them on a second output line” (emphasis added). Pain et al. does not disclose these limitations. To the contrary, Pain et al. discloses only two capacitors CLS and CLR, where capacitor CLS stores a single pixel signal and capacitor CLR stores a single reset signal. Pain et al. FIG. 2B. Applicant respectfully submits that Pain et al. does not combine a plurality of analog pixel and reset signals from a plurality of pixels as recited in claim 1. Since Pain et al. does not disclose all the limitations of claim 1, claim 1 and dependent claim 2 are not anticipated by Pain et al.

Claim 6, as amended, recites a binning circuit comprising, *inter alia*, a “first sample circuit storing a plurality of analog pixel signals from a plurality of pixels; [and a] second sample circuit storing a plurality of analog reset signals from a plurality of pixels” (emphasis added). Pain et al. does not disclose these limitations. To the contrary, Pain et al. discloses only two capacitors CLS and CLR, where capacitor CLS stores a single pixel signal and capacitor CLR stores a single reset signal. Pain et al. FIG. 2B. There is no first and second sample circuit storing a plurality of analog pixel and reset signals from a plurality of pixels as recited in claim 6. Since Pain et al. does not disclose all the limitations of claim 6, claim 6 is not anticipated by Pain et al.

Claim 10, as amended, recites a method of binning the output of an active image sensor comprising, *inter alia*, “sampling and combining analog output signals from a plurality of pixels of said sensor according to a first predetermined sequence; sampling and combining analog reset signals from a plurality of pixels of said sensor according to a second predetermined sequence” (emphasis added). Pain et al. does not disclose

these limitations. To the contrary, Pain et al. discloses only two capacitors CLS and CLR, where capacitor CLS stores a single pixel signal and capacitor CLR stores a single reset signal. Pain et al. FIG. 2B. Applicant submits that Pain et al. does not disclose sampling and combining analog output and reset signals from a plurality of pixels as recited in claim 10. Since Pain et al. does not disclose all the limitations of claim 10, claim 10 and dependent claims 13-14, 16, and 18 are not anticipated by Pain et al.

Claims 20 and 31, as amended, recite a charge-domain readout circuit comprising, *inter alia*, "a plurality of column readout circuits each of which sample and combine multiple pixel signals and reset signal values of a plurality of pixels of an active pixel sensor" (emphasis added). Pain et al. does not disclose this limitation. To the contrary, Pain et al. discloses only two capacitors CLS and CLR, where capacitor CLS stores a single pixel signal and capacitor CLR stores a single reset signal. Pain et al. FIG. 2B. There is no plurality of column readout circuits each of which sample and combine multiple pixel signals and reset signal values of a plurality of pixels as recited in claims 20 and 31. Since Pain et al. does not disclose all the limitations of claims 20 and 31, claims 20 and 31 are not anticipated by Pain et al. Claim 25 depends from claim 20 and is patentable at least for the reasons mentioned above.

Claim 26 recites a method of reading out values from active pixel sensors comprising, *inter alia*, "storing correlated double sampled values for a plurality of sensors in ... selected rows" (emphasis added). Pain et al. does not disclose this limitation. To the contrary, Pain et al. discloses only two capacitors CLS and CLR, where capacitor CLS stores a single pixel signal and capacitor CLR stores a single reset signal. Pain et al. FIG. 2B. There is no storing correlated double sampled values for a plurality of sensors in selected rows as recited in claim 26. Since Pain et al. does not disclose all the limitations of claim 26, claim 26 and dependent claims 27-28 are not anticipated by Pain et al.

Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection be withdrawn and claims 1-2, 6, 10, 13-14, 16, 18, 20, 25-28, and 31 be allowed.

Claims 1-14, 16, 18, 20-22, 24-28, and 31-33 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Sakurai et al. (US 6,850,278). This rejection is respectfully traversed.

Claim 1, as amended, recites an image sensor readout circuit comprising, *inter alia*, a "binning circuit [which] combines a predetermined plurality of analog pixel signals from a plurality of pixels and outputs them on a first output line, and combines a predetermined plurality of analog reset signals from a plurality of pixels and outputs them on a second output line" (emphasis added). Sakurai et al. does not disclose these limitations. To the contrary, Sakurai et al. discloses that "the signal Φ TX is set at high level to transfer signal charges from the photodiode PD.... A sensor signal S1 containing the noise signal N2 is ... accumulated in the capacitance CTS1 (first signal read-out). A sensor signal S2 containing the noise signal N1 is ... accumulated in the capacitance CTS2 (second signal read-out)." Col. 5, ln. 31-46 (emphasis added). Applicant respectfully submits that Sakurai et al. does not combine a predetermined plurality of analog pixel and reset signals from a plurality of pixels as recited in claim 1. Since Sakurai et al. does not disclose all the limitations of claim 1, claim 1 and dependent claims 2-5 are not anticipated by Sakurai et al.

Claim 6, as amended, recites a binning circuit comprising, *inter alia*, a "first sample circuit storing a plurality of analog pixel signals from a plurality of pixels; [and a] second sample circuit storing a plurality of analog reset signals from a plurality of pixels" (emphasis added). Sakurai et al. does not disclose these limitations. To the contrary, Sakurai et al. discloses that "the signal Φ TX is set at high level to transfer signal charges from the photodiode PD.... A sensor signal S1 containing the noise

signal N2 is ... accumulated in the capacitance CTS1 (first signal read-out). A sensor signal S2 containing the noise signal N1 is ... accumulated in the capacitance CTS2 (second signal read-out)." Col. 5, ln. 31-46 (emphasis added). There is no first and second sample circuit storing a plurality of analog pixel and reset signals from a plurality of pixels as recited in claim 6. Since Sakurai et al. does not disclose all the limitations of claim 6, claim 6 and dependent claims 7-9 are not anticipated by Sakurai et al.

Claim 10 recites a method of binning the output of an active image sensor comprising, *inter alia*, "sampling analog output signals from a plurality of pixels of said sensor according to a first predetermined sequence; sampling analog reset signals from a plurality of pixels of said sensor according to a second predetermined sequence; combining and outputting all sampled analog output signals on a first line; and combining and outputting all sampled analog reset signals on a second line" (emphasis added). Sakurai et al. does not disclose these limitations. To the contrary, Sakurai et al. discloses that "the signal Φ_{TX} is set at high level to transfer signal charges from the photodiode PD.... A sensor signal S1 containing the noise signal N2 is ... accumulated in the capacitance CTS1 (first signal read-out). A sensor signal S2 containing the noise signal N1 is ... accumulated in the capacitance CTS2 (second signal read-out)." Col. 5, ln. 31-46 (emphasis added). Applicant respectfully submits that there is no sampling and combining analog output and reset signals from a plurality of pixels as recited in claim 10. Since Sakurai et al. does not disclose all the limitations of claim 10, claim 10 and dependent claims 11-14, 16, and 18 are not anticipated by Sakurai et al.

Claims 20 and 31, as amended, recite a charge-domain readout circuit comprising, *inter alia*, "a plurality of column readout circuits each of which sample and combine multiple pixel signals and reset signal values of a plurality of pixels of an

active pixel sensor” (emphasis added). Sakurai et al. does not disclose this limitation. To the contrary, Sakurai et al. discloses that “the signal Φ TX is set at high level to transfer signal charges from the photodiode PD.... A sensor signal S1 containing the noise signal N2 is ... accumulated in the capacitance CTS1 (first signal read-out). A sensor signal S2 containing the noise signal N1 is ... accumulated in the capacitance CTS2 (second signal read-out).” Col. 5, ln. 31-46 (emphasis added). Applicant respectfully submits that Sakurai et al. does not sample and combine multiple pixel signals and reset signal values of a plurality of pixels as recited in claims 20 and 31. Since Sakurai et al. does not disclose all the limitations of claims 20 and 31, claims 20 and 31 are not anticipated by Sakurai et al. Claims 21-22 and 24-25 depend from claim 20 and are patentable at least for the reasons mentioned above. Claims 32-33 depend from claim 31 and are patentable at least for the reasons mentioned above.

Claim 26, as amended, recites a method of reading out values from active pixel sensors comprising, *inter alia*, “storing correlated double sampled values for a plurality of sensors in ... selected rows” (emphasis added). Sakurai et al. does not disclose this limitation. To the contrary, Sakurai et al. discloses that “the signal Φ TX is set at high level to transfer signal charges from the photodiode PD.... A sensor signal S1 containing the noise signal N2 is ... accumulated in the capacitance CTS1 (first signal read-out). A sensor signal S2 containing the noise signal N1 is ... accumulated in the capacitance CTS2 (second signal read-out).” Col. 5, ln. 31-46 (emphasis added). There is no storing correlated double sampled values for a plurality of sensors as recited in claim 26. Since Sakurai et al. does not disclose all the limitations of claim 26, claim 26 and dependent claims 27-28 are not anticipated by Sakurai et al.

Applicant respectfully requests that the 35 U.S.C. § 102(e) rejection be withdrawn claims 1-14, 16, 18, 20-22, 24-28, and 31-33 be allowed.

Claims 19 and 29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Pain et al or Sakurai et al. This rejection is respectfully traversed. Claim 19 depends from claim 10 and is patentable at least for the reasons mentioned above. Claim 29 depends from claim 26 and is patentable at least for the reasons mentioned above. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 19 and 29 be withdrawn.

Claims 15 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Pain et al or Sakurai et al. in view of Okamoto (US 2003/019580). This rejection is respectfully traversed. Claims 15 and 17 depend from claim 10 and are patentable over Pain et al. and Sakurai et al. at least for the reasons mentioned above. Okamoto, which has been cited as allegedly teaching sampling colors that take into account a Bayer pattern, fails to cure the above noted deficiencies of Pain et al. and Sakurai et al. Accordingly, Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 15 and 17 be withdrawn.

Claims 23 and 34-36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Pain et al in view of Admitted Prior Art (APA), presumably FIG. 3. This rejection is respectfully traversed. Claim 23 depends from claim 20 and is patentable over Pain et al. for at least the reasons mentioned above. Claims 34-36 depend from claim 31 and are patentable over Pain et al. for at least the reasons mentioned above. The alleged APA does not cure the above-noted deficiencies of Pain et al. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 23 and 34-36 be withdrawn.

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

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